Modeling and Co-Design of Novel Packaging Interposer with IPD Layers

Sung-Mao Wu [#1], Ting-Yao Wu [#2], Bo-Huie Yu [#3], Chen-Chao Wang[*4]

[#]*Micro Electrical Packaging Laboratory Department of Electrical Engineering, National University of Kaohsiung*
700, Kaohsiung University Rd., Nanzih District, 811. Kaohsiung, Taiwan
[1] sungmao@nuk.edu.tw
[2]dwtingyao@gmail.com
[3]dualbohuie@gmail.com

[*]*Electrical Laboratory, Corporation Design Division, Corporate R&D, Advanced Semiconductor Engineering (ASE) Inc., Kaohsiung, Taiwan*
No. 26, Chin 3rd Road, Nantze Export Processing Zone, Kaohsiung, Taiwan
[4]portal_admin@aseglobal.com

***Abstract* — Three innovation topics will be presented in this research. First, the structure of packaging interposer with IPD layers is proposed and broad-band equivalent model of TSV will be extracted too. Second, co-design case, coplanar waveguide transfer layers from top to bottom by TSV, is simulated by equivalent model we performed and compared with full wave EM simulation. Third, a resonator design with TSV, combining an inductor, a capacitor and the TSV model as well as second topic. The simulation results of the structure and equivalent model make us know the electrical characteristic of TSV and the extra effect of applied TSV.**

***Index Terms* — through silicon via, coplanar waveguide, resonator.**

I. Introduction

Today, the IC industries require the following points. To decrease the IC area, transform high speed and high frequency signals. Therefore, the third dimension IC was developed. The third dimension IC which means connecting the double side circuits both top and bottom. Unlike traditional IC has to connect each other side by side, third dimension IC could do the same thing up and down. So it could cut down the area of whole system IC. To make the way, we need to build a hole which pass through the silicon substrate for the double side circuits, that is the through silicon via (TSV) technology [1]-[3].

Through silicon via (TSV) technology is thought to be the essential technology of the next generation high-end semiconductors, 3-D packaging interposer for fan out the Input and Output (I/O) ports to outside package is one topic of it. TSV technology is proposed to solve the interconnect problem to reduce process area [4]-[7]. Because the package has lot of effect to the circuit, there needs several solutions to fix it. So, we will need to set up some circuits to the path from IC to load board. When we make those circuits, the electrical character should be considered

Therefore, we discuss the electrical character of TSV, and proposed the model of the TSV, and we also make several examples and create the model for each example to check the model is useful.

II. Structure and Modeling

Figure 1 shows the novel structure of interposer with IPD layers. It consists of dielectric layers, through silicon via and three redistribution layer. Top redistribution layer (RDL1), and two redistribution layers below the silicon substrate (RDL2 & RDL3) were Copper. The dielectric layers (BCB1 to BCB5) were SINx. The thickness of each layer is shown in table.I. The integrated passive components circuit could be designed in Copper layers (RDL1.RDL2.RDL3).

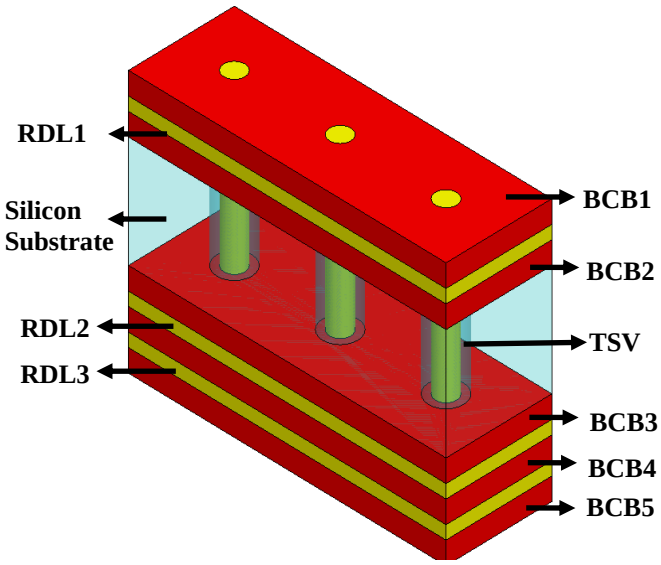

Fig.1 Novel Structure of Interposer with IPD Layers.

TABLE I
THE THICKNESS OF EACH LAYER

Layer	Thickness	Layer	Thickness
BCB1	5 μm	Silicon	150 μm
M1	3 μm	BCB4	3 μm
BCB2	5 μm	M3	3 μm
M2	3 μm	BCB5	5 μm
BCB3	5 μm		

The equivalent model of TSV in packaging interposer can be established by transmission line theorem. Figure 2 shows the simulation structure and proposed equivalent model of TSV by transmission line theorem [8]. The structure we used to simulate is Ground-Signal-Ground (GSG), including three through via, one for signal, and two for grounding. Two exciting ports, port1 and port2, are placed in RDL1 and RDL2 layers, typical TSV length when co-design with IPD circuits.

By the equivalent model shows in Figure 2, unbalance RLCG model of transmission line is used to perform TSV model. Series resistance (RofTSV) and series inductance (LofTSV) in the middle of the model present the trace loss and magnetic flux of grounding-return paths of TSV individually. And shunt capacitance (Csil) presents electric coupling between each TSV or to ground capacitance. This equivalent model is made to simulate the electrical characterization of TSV and used to co-design with IPD later.

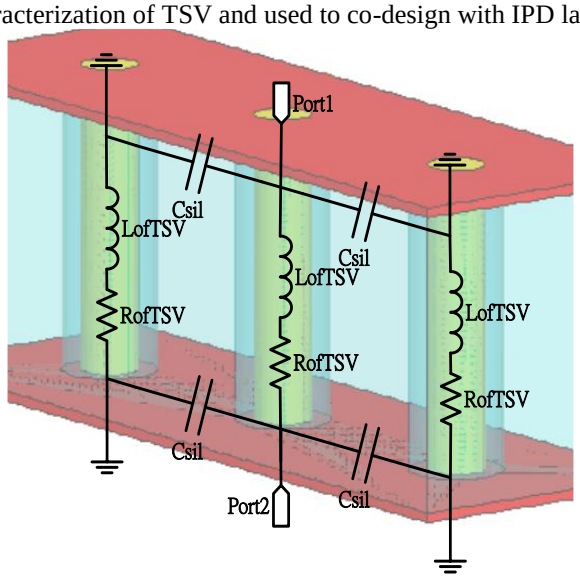

Fig.2 Equivalent Model of TSV in GSG Type

To find correct equivalent model of TSV [9], full wave 3D EM simulation result is extracted to perform broad band equivalent model of TSV, each parasitism values of model components are shown in Table II.

TABLE II
THE PARASITISM VALUES OF MODEL COMPONENTS

Component name	Value
Csil	3 fF
LofTSV	0.25 nH
RofTSV	6 mOhm

Once we created the equivalent model, we made the simulation of the model to find the S parameter and phase. Figure 3 and figure 4 show the comparison result between the TSV structure and the equivalent model. In these figures, we could discover that the results both 3D structure EM simulation and equivalent model to correspond exactly.

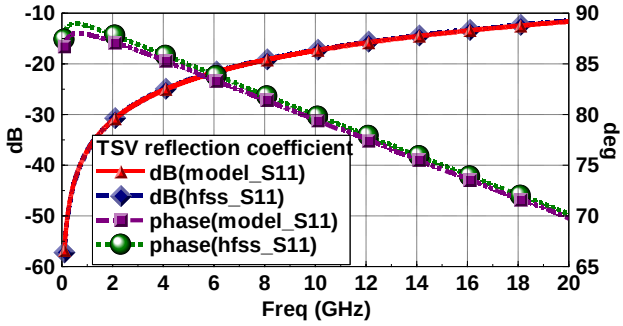

Fig.3 Compare Reflection Coefficient of the 3D EM Structure Simulation and the Equivalent Model

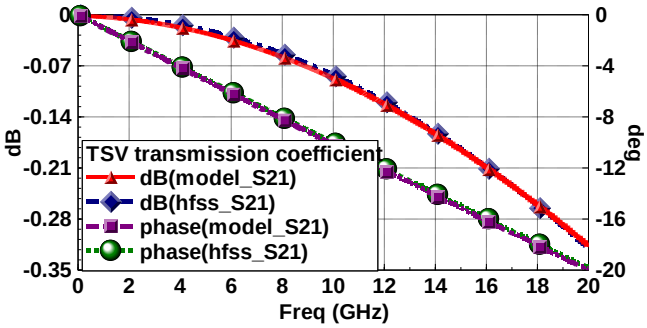

Fig.4 Compare Transmission Coefficient of the 3D EM Structure Simulation and the Equivalent Model

III. CO-DESIGN EXAMPLE OF CPW-TSV-CPW

For verify the model of TSV correct or not and perform IPD co-design characterization, a interposer with IPD co-design structure, coplanar waveguide transfer layers from top to bottom by TSV, is created and simulated. Figure 5 shows the full structure of CPW-TSV-CPW.

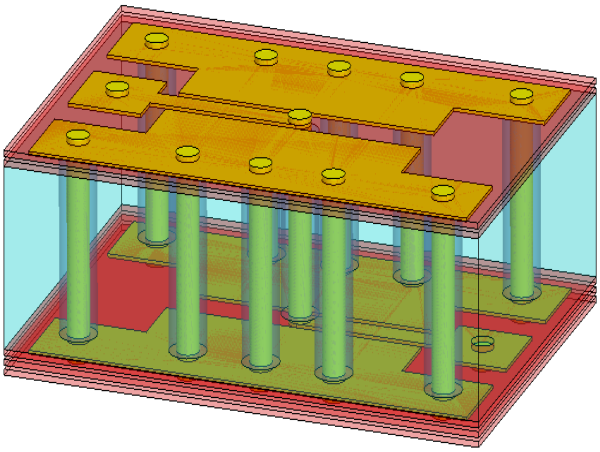

Fig.5 Structure of CPW-TSV-CPW

First, we create the CPW model by simulating the electrical characterization of CPW. Figure 6 shows the model of CPW, series resistance (Rc) and series inductance (Lc) in the middle

of the model present the trace loss and magnetic flux of grounding-return paths of CPW individually. And shunt capacitances (Cg) presents electric coupling to ground capacitance, another shunt capacitances.(Cp) present the pad effect. And the parasitism value of CPW model components shows in table III. Second, we combine the models of CPW and TSV.

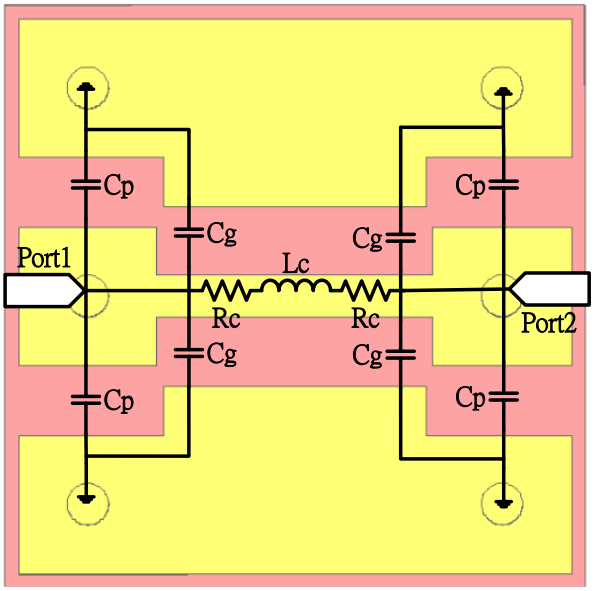

Fig.6 Model of CPW

TABLE III
THE PARASITISM VALUES OF CPW MODEL COMPONENTS

Component name	Value
Cp	20 fF
Cg	11 fF
Rc	6 mOhm
Lc	0.29 nH

At last, compare with the simulation result between model and 3D EM simulation. Figure 7 and Figure 8 show the simulation result comparison with EM extracting by the CPW-TSV-CPW structure and circuit simulation by TSV equivalent model. Curve is fit and very similar or equal exactly, too.

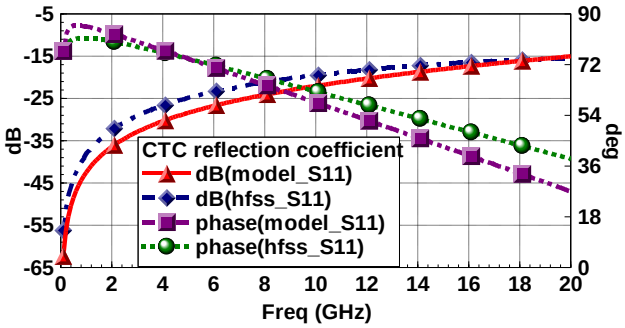

Fig.7 Compare Reflection Coefficient of the C-T-C Structure and the Equivalent Model

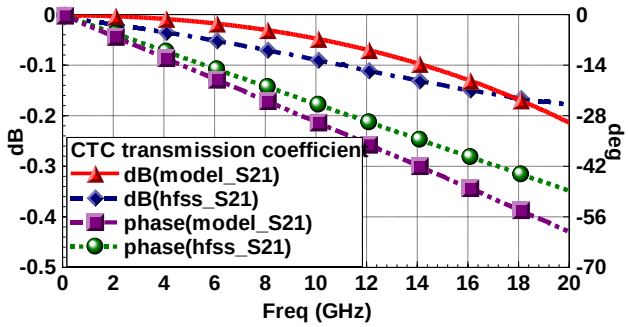

Fig.8 Compare Transmission Coefficient of the C-T-C Structure and the Equivalent Model

IV. CO-DESIGN EXAMPLE OF RESONATOR

Further, we design resonator by using inductor and capacitor. On the structure, RDL1 layer is used as inductor, and capacitor is proposed between RDL2 and RDL3 layer. These layers are connected by TSV. Figure 9 shows the full structure of resonator.

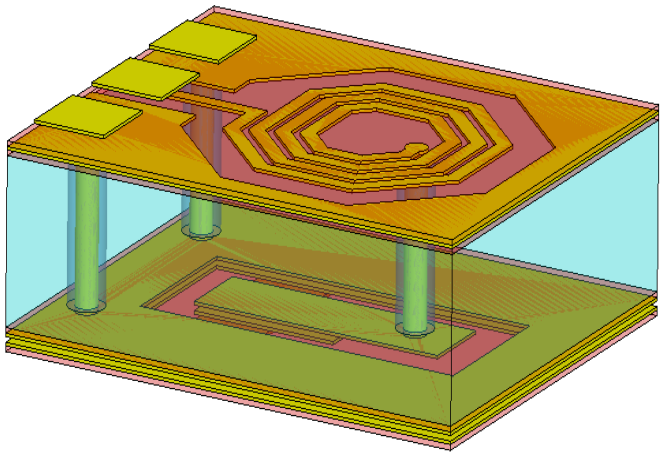

Fig.9 Structure of Resonator

Before we propose entire structure, we create the individual model of inductor and capacitor with the simulation of their structure. Then, we consider the effect of pad, and do the de-embedding to eliminate this effect. Next, we simulate the electrical characterizations after integrating three models, inductor, TSV and capacitor. Figure 10 shows the full model of the structure. In the layer RDL1, shunt capacitances (Cg1) presents electric coupling to ground capacitance, the series resistance (Rl) presents the loss on path, and the series components that shunt an inductance (Ll) and a capacitance (Cl) in the center present the magnetic flux and coil coupling. In the layer RDL2 and RDL3, shunt capacitances (Cg2) presents electric coupling to ground capacitance. Series resistance (Rc) and inductance (Lc) present the trace loss and magnetic flux of grounding-return paths of capacitor individually, and capacitance (Cc) in the middle presents the electric between two parallel-plates. Table 4 shows the parasitism values of full resonator model.

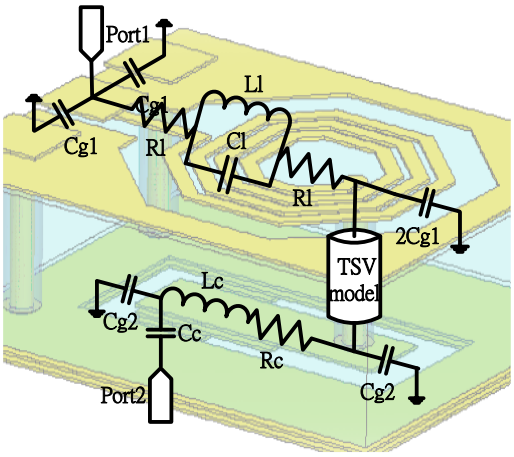

Fig.10 Model of Full Structure

TABLE IV
THE PARASITISM VALUES OF RASONATOR MODEL COMPONENTS

Name	Value	Name	Value
Cg1	30 fF	Cg2	20 fF
Rl	20 mOhm	Rc	16 Ohm
Cl	10 fF	Lc	145 pH
Ll	3 nH	Cc	109 fF

At last, we compare simulation result of structure and the equivalent model. Because the TSV grand via has been set up farther than before, so we change capacitance of electrical coupling between each TSV. Figure 11 and figure 12 shows the result of the comparison.

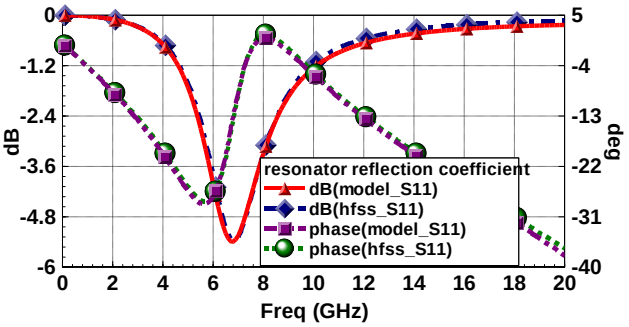

Fig.11 Compare Reflection Coefficient of the Resonator Structure and the Equivalent Model

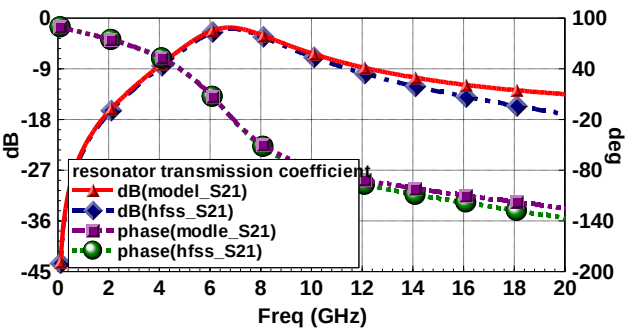

Fig.12 Compare Transmission Coefficient of the Resonator Structure and the Equivalent Model

VI. CONCLUSION

In this study, we presented the equivalent model by transmission line theorem in TSV, verified it by co-design case and design a resonator to test the electrical characterization of TSV for application. Although we only have simulation results and don't have relative process technology, we can use simulation result to predict the electrical characterization of TSV. Therefore, we don't have any measurement results in this paper. The TSV can replace the vertical connection in PCB or 3D IC. This way can decrease the area of PCB board and reduce the transmission path. In the future, the goals of the slight, thin and small product can be achieved.

REFERENCES

[1] T. Whipple, T. Kukal, K. Felton, V. Gerousis" IC-Package Co-design and Analysis for 3D-IC Designs," in IEEE 3D System Integration, 2009, pp.1-6.

[2] S. Fujita, K. Abe, K. Nomura, S. Yasuda and T. Tanamoto" Perspectives and issues in 3D-IC from designers' point of view" in IEEE Circuit and System, 2009, pp.73-76.

[3] P. Falkenstern, Y. Xie, Y. W. Chang, Y. Wang" Three-Dimensional Integrated Circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis," in ASP-DAC, 2010, pp.169-174.

[4] S. W. Yoon, D. W. Yang, J. H. Koo, M. Padmanathan and F. Carson "3D TSV Processes and its Assembly/Packaging Technology," in IEEE 3D system Integration Conf. 2009, pp.1-5

[5] P. Kettner, B. Kim, S. Pargfrieder, S. Zhu "New Technologies for advanced high density 3D packaging by using TSV process," in IEEE Conf. 2008, pp.1-3.

[6] Al-sarawi, D. Abbott, and P. D. Franzon, "A Review of 3-D Packaging Technology" in IEEE Components, Packaging, and Manufacturing Technology, 1998, pp. 2-14.

[7] J. S. Pak, C. Ryu, J. Kim, Y. Shim, G. Kim, and J.Kim "Wideband Low Power Distribution Network Impedance of High Chip Density Package using 3-D Stacked Through Silicon Vias," in Asia-Pacific microwave conf. 2006, pp. 1855 – 1858.

[8] J. Kim, E. Song, J. Cho, J. S. Pak, J. Lee, H. Lee, K. Park and J. Kim "Through Silicon Via (TSV) Equalizer," in IEEE Electrical Performance of Electronic Packaging Conf. 2009, pp.13-16.

[9] .C. Ryu, D. Chung, J. Lee, K. Lee, T. Oh, and J. Kim "High Frequency Electrical Circuit Model of Chip-to-Chip Vertical Via Interconnection for 3-D Chip Stacking Package," in IEEE Electrical Performance of Electronic Packaging Conf. 2005,pp.151-154.