A CMOS Inverter Detector for Package High-Speed Characteristics Testing

Wei-Chi Chen,Yu-Yung Wu,Yuan-Ming Wu, Sung-Mao Wu
Department of Electrical Engineering, National University of Kaohsiung
No. 700, Kaohsiung University Road, Nan-Tzu District, Kaohsiung, 81148, Taiwan, R.O.C.
Phone: +886-7-5919436, Fax: +886-7-5919374, E-mail: sungmao@nuk.edu.tw

Abstract

In high speed and high frequency, SSN would be found in transistor switching. Switching current would be produced when I/O port operator in the same time. In this paper, an inverter circuit is designed in high frequency and high speed environment. Simultaneous switching noise (SSN) and signal-integrity problem would be found in package. This research designs an inverter chip and BGA structure on package. It can be obtained different voltage-transfer characteristic from noise margins and amplitude diversification from time domain

Introduction

In recent years, with the rapid development of wireless communication industry, all of the wireless communication products are dedicated on slim, light, high speed and high performance. Thus, the ICs become smaller and the operating frequency getting higher, the package will be important role. Package path length relative to the chip length of the line is very long. In the high frequency the power integrity (PI) /signal integrity (SI) problems become important, such as simultaneous switching noise (SSN).

The PI problem causes amplitude diversification by square wave. Square-wave is compared with packing chip and chip only by signal output. The signal loss and phase shift shows that the package increases the resistance, inductance, and capacitance.

The SSN problem causes digital signal produce error operator by voltage level drift. Inverter is a testing chip for this problem. The transistor is conducted by instant current. It causes parasitic inductance on return current path, called transient voltage. The transient voltage produces between power layer and ground layer on package, called SSN. By comparing the inverter output noise margins and amplitude diversification, use result to develop SSN effects on package.

In this research, inverters operating at high frequency and high speed module are realized by TSMC 0.18μm MOSFET process [1]. An inverter circuit is designed in high frequency and high speed environment. Simultaneous switching noise (SSN) and signal-integrity problem would be found in package. This research designs an inverter chip and BGA structure on package. Switching current would be produced when I/O port operator in the same time. By building the mode of package IP and combine with the chip the find package effect.

Means of Package Testing

A circuit is proposed to measure the packaging effect. To achieve this target, inverters and switches are designed in the chip. By comparing the different between the loaded and unloaded of package, the effect of the package would therefore obtain.

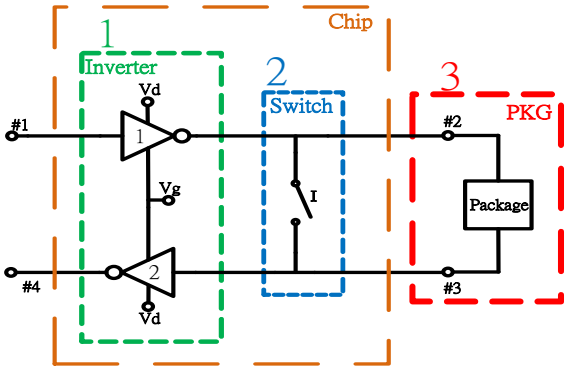


Fig. 1 The concept of the design

Fig. 1 shows the concept of the design. It can be divided into three parts. Part one is a two-level inverter, making the input signal and output signal in the same level. The bias voltage, Vd and Vg, are 1.6V and 1V respectively [5].

Second part is the switch. Step 1, the Square wave of inverter is applied by measurement (chip only) to confirm the original waveform on package. Step 2, closing switch I change the way to provide the amplitude diversification on package (chip with PKG). Via this design, the packaging effect is therefore shown.

Apart from the chip including the first and second part, testing package of the third part is made on the substrate. It consists of wire bond, via, and transmission line, etc.

Fig. 2 is the inverter circuit. The inverter is designed by two MOSFET models. Q1 is designed as load and Q2 is where signal is active. In order to prevent the interrupting of source, adding a capacitor as DC block. To avoid signal interfering the DC input, an inductor is added as RF choke [2].

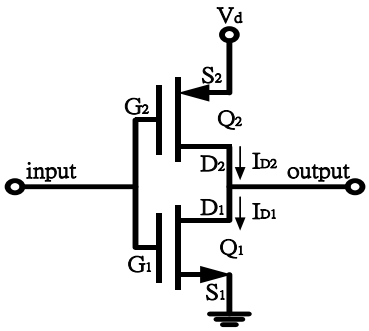


Fig. 2 The inverter circuit

The switch circuit controls the signal's direction. The signal only goes through inverters when higher voltage level is given to switch. The signal goes through the package when switch I is at lower voltage level.

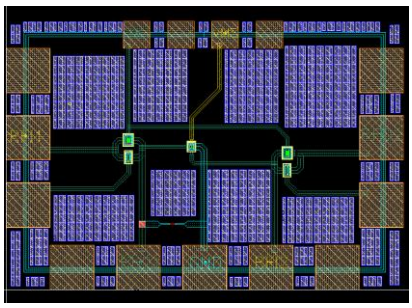
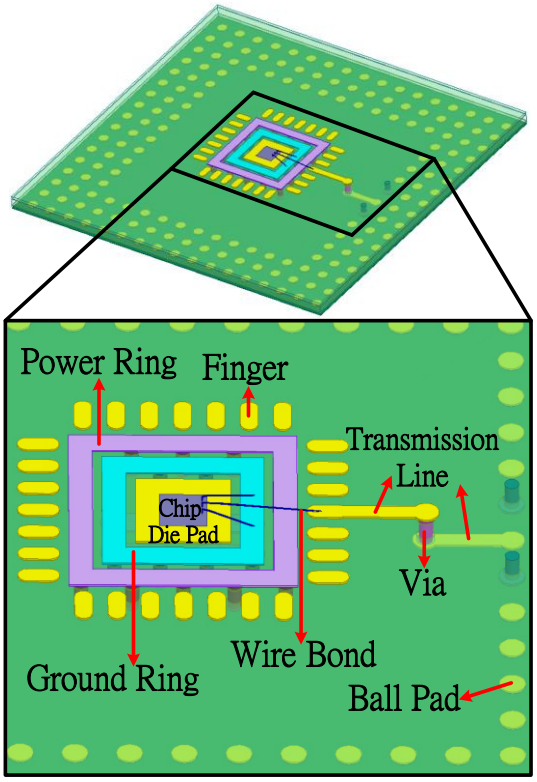


Fig. 3 The layout of the chip.

The layout of the chip is shown in Fig. 3. TSMC 0.18μm MOSFET process is used to design the inverters and switches.

The BGA design is shown in Fig. 4. The chip is designed on four layers package substrate. Testing signal goes through the wire bond, transmission line and via to the chip from the bottom layer. Metal material is copper, and dielectric materials are FR-4 and PP. Spurious effect is shown at high frequency. As a result, the package will seriously affect the circuit performance.

At the high frequency, the package generate the transmission line effects, and cause the signal loss,



delay. The simulation results can establish the RLC equivalent model, and further analysis the signal incomplete.

Fig. 4 The BGA design for inverter testing

Result and Discussion

The testing amplitude diversification can divide into two steps. Step 1, the Square wave of inverter is applied by measurement (chip only) to confirm the original waveform on package. Step 2, closing switch I change the way to provide the amplitude diversification on package (chip with PKG).

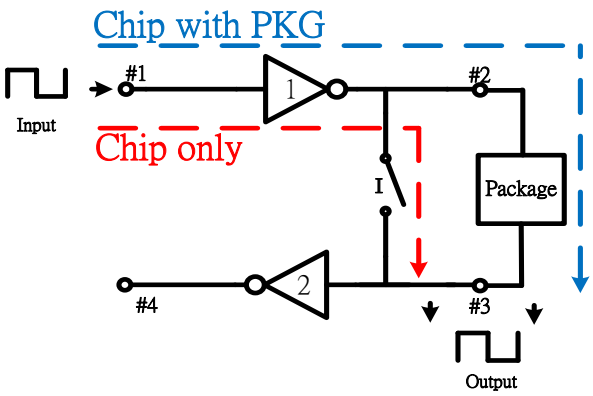


Fig. 5 The signal path of Chip with PKG and Chip only

In Fig. 6 the output square wave on chip with package and chip only is compared. Based on Fig.7, the signal loss and phase shift shows that the package increases the resistance, inductance, and capacitance.

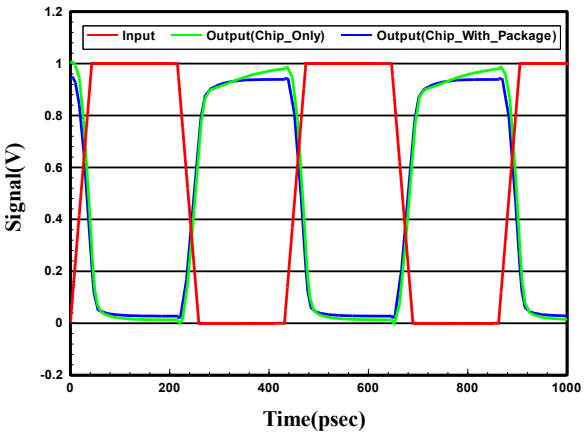


Fig. 6 The square wave of input and output

The noise margin express from eq. (1) and (2).

$$NM_L = V_{IL} - V_{OL} \quad (1)$$

$$NM_H = V_{OH} - V_{IH} \quad (2)$$

Fig. 7 shows voltage transfer curve. It expresses the voltage of high voltage level to low voltage level. When the voltage difference gets lower, the signal will cause noise interference. The signal goes through the package and makes the low voltage higher. It causes the high level and low level voltage getting closer, which would influence the performance of inverters.

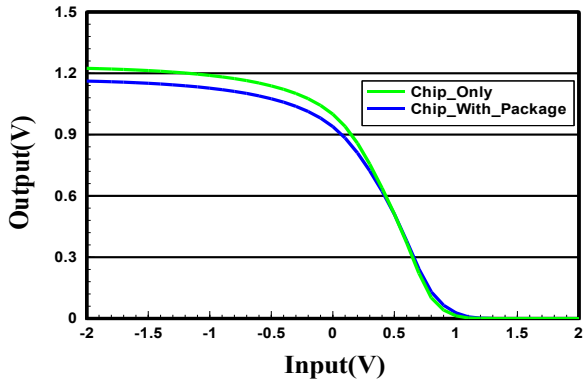


Fig. 7 The voltage transfer characteristic of the CMOS inverter

TABLE I NOISE MARGIN

	Chip only (v)	Chip with PKG (v)
NMH	**0.058**	**0.099**
NML	**0.0412**	**0.158**

Conclusion

In this research, the inverter chip is going to be fabricated by TSMC CMOS 0.18μm technology. In the future, verification of measurement by this chip and the designed package will be realized. The models extract from package by voltage-transfer characteristic of noise margins and amplitude diversification of time domain to develop package IP technology to reduce the time of chip and package co-design.

Acknowledgement

This work is supported under grant NSC-100-2221-E-390-028 from National Science Council of R.O.C. The authors are grateful to Bureau of Standards, Metrology & Inspection, M.O.E.A., R.O.C. for providing all necessary support.

References

[1] Zhangcai Huang; Kurokawa, A.; Hashimoto, M.; Sato, T.; Minglu Jiang; Inoue, Y; "Modeling the Overshooting Effect for CMOS Inverter Delay Analysis in Nanometer Technologies," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol.29, no.2, pp.250-260, Feb. 2010.

[2] Dhar, B.M.; Ozgun, R.; Jung, B.J.; Katz, H.E.; Andreou, A.G.; , "Optimum bias of CMOS organic field effect transistor inverter through threshold adjustment of both p- and n-type devices," Electronics Letters , vol.46, no.19, pp.1335-1336, Sept. 16 2010.

[3] Le, T.T.; Yu, H.Y.; Sun, Y.; Singh, N.; Zhou, X.; Shen, N.; Lo, G.Q.; Kwong, D.L.; , "High-Performance Poly-Si Vertical Nanowire Thin-Film Transistor and the Inverter Demonstration," Electron Device Letters, IEEE , vol.32, no.6, pp.770-772, June 2011.

[4] Tang, X.; Pun, K.-P.; ,"High-performance CMOS current comparator," Electronics Letters , vol.45, no.20, pp.1007-1009, September 24 2009.

[5] Chunsheng Shao; , "Analysis for Manufacturing Process Flow of 0.18μm CMOS Inverter," Journal of Changzhou Institute of Technology,vol.22,no.1/2,April 04 2009.

[6] Iizuka, T.; Nakura, T.; Asada, K., "Buffer-ring-based all-digital on-chip monitor for PMOS and NMOS process variability and aging effects," Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2010 IEEE 13th International Symposium on , pp.167-172, 14-16 April 2010.